

Low Power High Speed Folded Cascode Amplifier With PMOS Inputs

B. Krishna M.Tech(VLSI), D. Arun kumar M.E(Embedded systems & VLSI Design)
 Asst.Prof,Dept of ECE KITE Womens College of Professional Engineering Sciences-SHABAD
 Asst.Prof,Dept of ECE KITE Womens College of Professional Engineering Sciences-SHABAD

Abstract

This paper presents the design of low power high speed folded Cascode amplifier with PMOS inputs. The design is carried out using **LTSPICE** tool in **180 nm** CMOS technology.

I. Introduction

The main aspects of folded Cascode amplifier design are high DC gain, high slew-rate, and high band width. The chosen topology is of PMOS input type and the bias circuit for the proper operation of the circuit is designed. The power supply here is constrained to $\pm 1.65V$ and the technology used is 180nm.

Specifications of Folded Cascode Opamp:

Parameter	Value
Technology	180 nm
Power supply	$\pm 1.65 V$
Gain	>50 dB
Slew rate	150 V/ μ sec
Unity gain bandwidth	150 MHz
Phase margin	>60 degrees
Power consumption	< 5 mW
PSRR	>60 dB
Offset voltage	-

Table 1. Specifications of Folded Cascode op-amp

II. Proposed Topology

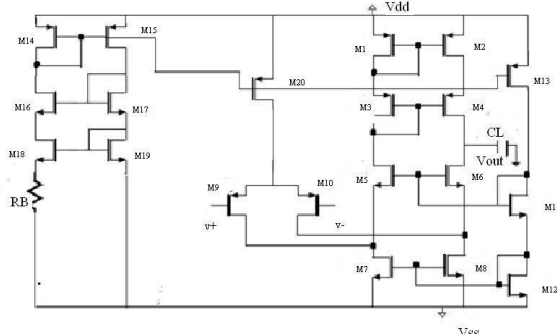


Fig 1.Folded Cascode with PMOS inputs

III. Design Calculations

We know that,

$$I_{bias} = SR \times C_L = 150 \times 10^6 \times 10^{-12} = 150 \mu A$$

$$\text{Transconductance, } gm = 2\pi \times (GBW) \times CL = 0.942 \text{ m-S}$$

We know that,

$$gm = \sqrt{2Kp \left(\frac{W}{L}\right) I_{bias}} \quad S$$

Open loop voltage gain of folded cascode Opamp is given by

$$A_v = (gm9 \cdot gm4 \cdot gm6) / \{I_D^2 (gm4 \cdot \lambda_N^2 + gm6 \cdot \lambda_P^2)\}$$

where, $gm9$, $gm4$, $gm6$ are the transconductance of the transistors M_9 , M_4 , M_6 respectively and λ_N and λ_P are the channel length parameters of NMOS and PMOS respectively. Taking the complementarity between the M_6 and M_4 ,

$$gm6 = gm4$$

Now the gain expression becomes,

$$A_v = gm9 \cdot gm4 / I_D^2 (\lambda_N^2 + \lambda_P^2)$$

From the above equation calculate, "W" which is found to be $17 \mu m$ which is the size of input transistors. Similarly the second stage in the topology has the bias current of $150 \mu A$ from which we can calculate the remaining aspect ratios of all MOS transistors.

$$W9 = W10 = 17 \mu m$$

$$W1 = W2 = W3 = W4 = 14 \mu m$$

$$W5 = W6 = W7 = W8 = 5 \mu m$$

$$W11 = W12 = 5 \mu m.$$

Constructing the bias circuit of an Op-amp to provide the required bias current. Transistor transconductance is the most important parameters in Opamp that must be stabilized. In general biasing of an Opamp is to ensure the proper operation of the circuit.

From the above circuit, writing KVL for the bottom loop in the bias circuit,

$$V_{gs19} = V_{gs18} + I_{D18} \cdot R_B$$

$$\text{And we know, } V_{eff} = V_{gs} - V_t$$

$$V_{eff19} = V_{eff18} + I_{D18} \cdot R_B ; (W/L)_{14} = (W/L)_{15} \quad \&$$

$$I_{D18} = I_{D19}$$

$$\sqrt{2 \frac{I_{D19}}{K_n (W/L)_{19}}} = \sqrt{2 \frac{I_{D18}}{K_n (W/L)_{18}}} + I_{D18} \cdot R_B$$

$$\frac{2}{\sqrt{2 I_{D19} K_n (W/L)_{19}}} \left\{ 1 - \frac{\sqrt{(W/L)_{19}}}{\sqrt{(W/L)_{18}}} \right\} = R_B$$

We know,

$$g_{m19} = \sqrt{2 K_n (W/L)_{19} I_{D19}}$$

$$\frac{2}{g_{m19}} = \frac{R_B}{\left\{ 1 - \frac{\sqrt{(W/L)_{19}}}{\sqrt{(W/L)_{18}}} \right\}}$$

$$g_{m19} = \frac{2}{R_B} \cdot \left\{ 1 - \frac{\sqrt{(W/L)_{19}}}{\sqrt{(W/L)_{18}}} \right\}$$

From the above expression it is to be noted that aspect ratios of M18 and M19 should never be the same. For the special case,

$$\left(\frac{W}{L}\right)_{18} = 4 \left(\frac{W}{L}\right)_{19}$$

Therefore, $g_{m19} = 1/R_B$

So, simply the trans-conductance depends on the resistance R_B . Adjust this R_B to obtain your required biasing current.

Aspect ratios of the MOS transistors are as follows:

$$W_{14} = W_{15} = W_{16} = W_{17} \text{ \& } W_{18} = 4W_{19}$$

IV. Simulation results of Folded Cascode Opamp

Gain and Phase plot

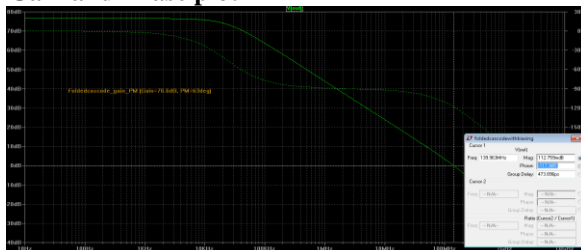


Fig 2 Gain and Phase plots of Folded Cascode Opamp with biasing circuit

Input Common Mode Range (ICMR):

For the calculation of ICMR, connect the Opamp in feedback and apply a ramp input to the non-inverting terminal and perform the transient analysis, the output is plotted as shown in below fig

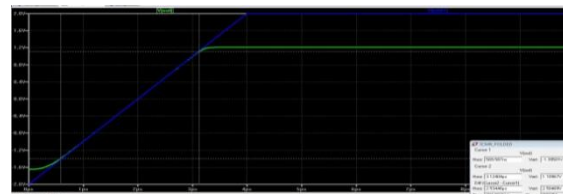


Fig 3 Plot shows ICMR result of Folded Cascode Opamp

From the above graph, the common mode input range is found to be -1.39V to 1.10V.

Slew rate (SR):

Slew rate of an Op amp is defined as the maximum rate of change of output for the small change in input

$$SR = \left[\frac{dV_o}{dt} \right]_{\max}$$

Generally SR is determined from the slope of output waveform during rise or fall of the output when the input is applied. So, we have a positive SR and a negative SR

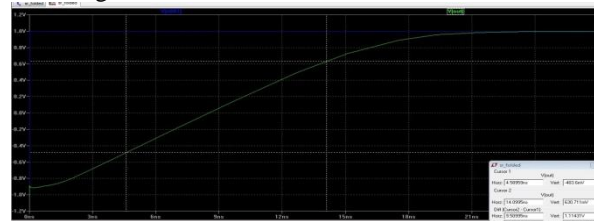


Fig 4 Positive Slew rate of Folded Cascode Opamp

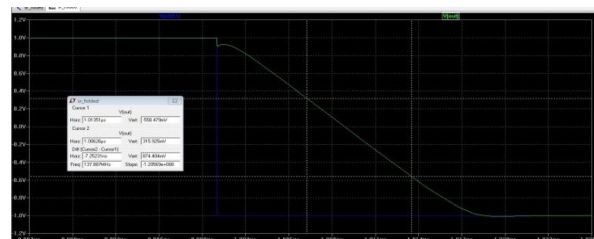


Fig 5. Negative Slew rate of Folded Cascode Opamp

From the above graph it is inferred that positive SR = 117 V/μsec
 And negative SR = -120 V/μsec

V. PSRR of a Folded Cascode Opamp:

PSRR performance of an Opamp can be found by applying a small sinusoidal signal to the power supply

$$PSRR = 20 \log(V_{out}/V_{in})$$

The following fig. shows the graph of PSRR. In general, this value should be as high as possible over a wide range of frequency.

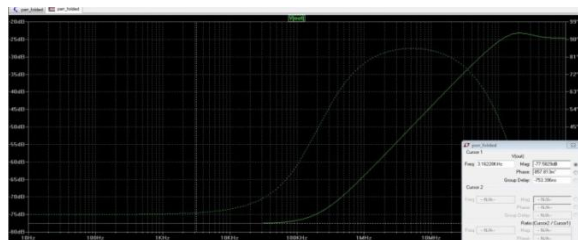


Fig 6 PSRR of Folded Cascode Opamp

Positive PSRR=77dB
Negative PSRR=104 dB

Power dissipation

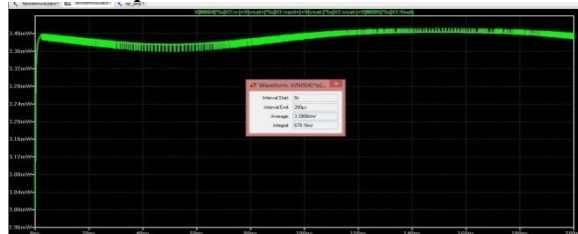


Fig 7 Power dissipation of folded cascode op-amp

VI. Summary of folded cascode op-amp

Parameter	Value
Gain	77 dB
Phase Margin	63 degrees
Unity frequency(UGF)	gain 140 MHz
Offset voltage	31 μ v
SR+	117 V/ μ s
SR-	-120 V/ μ s
PSRR+	77 dB
PSRR-	104 dB
ICMR	-1.39 V to 1.10V
Power dissipation	3.39 mW

Table 2 Summary of folded Cascode op-amp

VII. Conclusions

In this thesis, a Low power high speed folded Cascode op-amp capable of providing high gain(77dB) and High speed with more stable(Phase margin=63) is designed in **LTSPICE with 180nm CMOS technology**. Simulation results are observed that circuit dissipates very low power.

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VIII. About Authors



Mr.B.Krishna

completed **B.Tech** in ECE From Dr.Paul-Raj Engineering College Bhadrachalam(JNTUH) in 2005 and **M.Tech(VLSI-SD)** From SITAMS-Chittoor(JNTUH) in 2008. Presently he is working in **KITE Womens College of Professional Engineering Sciences** as a **Asst. Professor**



Mr. D.Arunkumar-Graduated(B.Tech) from Vaagdevi College Of Engineering in Electronics and Communication Engineering and **Master in Engineering** from Vasavi college of Engineering in Embedded Systems and VLSI Design. Presently he is working in **KITE Womens College of Professional Engineering Sciences** as a **Asst. Professor**